REMARKS/ARGUMENTS

Claims 1 – 20 are pending in this application. Claims 1 – 15 are withdrawn from consideration. Claims 16 - 20 are rejected under 35 USC § 102(b). New claims 21 – 32 have been added. No new matter has been added. In view of the following remarks, reconsideration and allowance of all pending claims are respectfully requested.

Election Restriction

Claims 1-15 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a non-elected invention, there being no allowable generic or linking claim. Applicant traversed the restriction requirement in a reply filed on July 29, 2005. The Examiner has not found the Applicant's traversal persuasive and deemed the restriction final.

Claim Rejections under 35 U.S.C. § 102(b)

Claims 16 – 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,177,787 to Hobrecht.

Applicant believes that at least the following limitation is not taught by any of the cited references as are found in Applicant's claim 16: "adjusting a slope associated with a ramp signal in response to the measurement signal".

According to the Office Action, the Hobrecht reference discloses "providing a measurement signal [via control circuit 304] that is associated with the measured parameter" and "adjusting a slope [shown in FIG. 5] associated with a ramp signal in response to the measurement signal". It is somewhat unclear as to which signal from FIG. 5 of Holbrect is identified as a "ramp signal". The only conceivable ramp signals from FIG. 5 of Holbrect are

identified as signals 524 and 526, namely the integration current signal (I_{INT}) and the capacitor voltage signal (V_C).

Applicants have reviewed the schematics of FIG. 2 and the related description in the detailed description of Holbrect for an understanding as to the operation of integration current signal (I_{INT}) and capacitor voltage signal (V_C). The current from a DAC circuit (202) is used to control the integration current signal (I_{INT}) by changing the amount of current that is drawn through capacitor 222. The capacitor voltage signal (V_C) is developed by accumulating charge when the integration current signal (I_{INT}) is flowing from the operational amplifier (224). Periodically, the capacitor is discharged when the RESET signal is asserted. Quite interestingly, the DAC circuit (202) is controlled by a digital counter (208), which is **ONLY** responsive to digital control signals FC/2, PH1 and PH3. The digital counter and the capacitor are both reset by the RESET signal in response to signals PH1 and PH3, while the counter will only change states when triggered by a rising edge of signal FC/2.

Applicant's have reviewed the schematics of FIG. 1 and the related detailed description of Holbrect for a better understand the operation and timing of signals FC/2, PH1 and PH3. FIG. 1 illustrates a timing control circuit (100) that generates signals PH1 - PH6 and FC/2 from a single input signal, namely the master clock signal FC. Quite simply, signal FC/2 is a clock signal that is generated by dividing the master clock signal in two, and signals PH1 – PH6 are generated by a counter that increases in value based on the signal FC/2. As such, none of the signals PH1 – PH6 and FC/2 are responsive to any signals with the exception of the master clock signal FC.

Referring again to FIG. 2 of Holbrect and the related description, the digital counter 208 is arranged to count in response to FC/2, which is related to the master clock signal divided by two. A careful review of FIG. 5 confirms that signal 524, the integration current signal (I_{INT}) changed over time in response to rising edges of signal 502 (FC/2). Moreover, the capacitor voltage signal (V_C) of FIG. 5 provides a charging time that is determined by the integration current signal 524, and changes in synchronization therewith.

Referring again to Applicant's claim 16, "measuring a parameter associated with the inductor", "providing a measurement signal that is associated with the measured parameter",

and "adjusting a slope associated with a ramp signal **in response to the measurement signal** (emphasis added)" is simply not found in the Hobrecht reference. None of the conceivable "ramp signals" from Hubert's FIG. 5 is response to the measurement signal as described in Applicants claim 16. As such a notice of allowance with respect to claim 16 is respectfully requested. Claims 17 and 18 depend upon and further limit claim 16, and should be allowed for that reason as well as any other limitations they recite. Claims 16 – 18 are proposed to be allowable and notice to that effect is requested.

Applicant believes that at least the following limitation is not taught by any of the cited references as are found in Applicant's claim 19: "a means for adjusting a slope that is associated with a ramp signal in response to the measurement signal". Claim 19 contains similar limitations as that described with respect to claim 16 in that the adjustment of the slope of the ramp signal in Applicants' claim 19 is responsive to the measurement signal as previously discussed. For at least those reasons described above with respect to claim 16, claim 19 is proposed to be allowable and notice to that effect is requested. Claim 20 depends upon and further limits claim 19, and should be allowable for that reason as well as any other limitation recited. Claims 19 – 20 are proposed to be allowable and notice to that effect is requested.